

Frequency Synthesizer

for UHF telecommunication systems, e.g. cellular radio and cordless telephone

Description / Technology

The programmable frequency synthesizer IC U2780B for μP controlled application is realized with a high speed BI-POLAR technology which is very suitable for combinations of fast ECL logic and low current I^2C logic. The benefits are high input sensitivity in connection with low power consumption and therefore small packages (SSO-20).

This feature makes the device very suitable for cordless phones and handheld cellular radio sets up to 1.1 GHz.

The IC is controlled by a 3-wire-bus with the inputs for Clock, Data and Enable for programming the scaling fac-

tors of the programmable counter, the reference counter and the prescaler.

A TCXO can be connected to the oscillator input (OSCin) as an alternative solution to the common crystal reference oscillator. In that case the oscillator output (OSCout) should be left open.

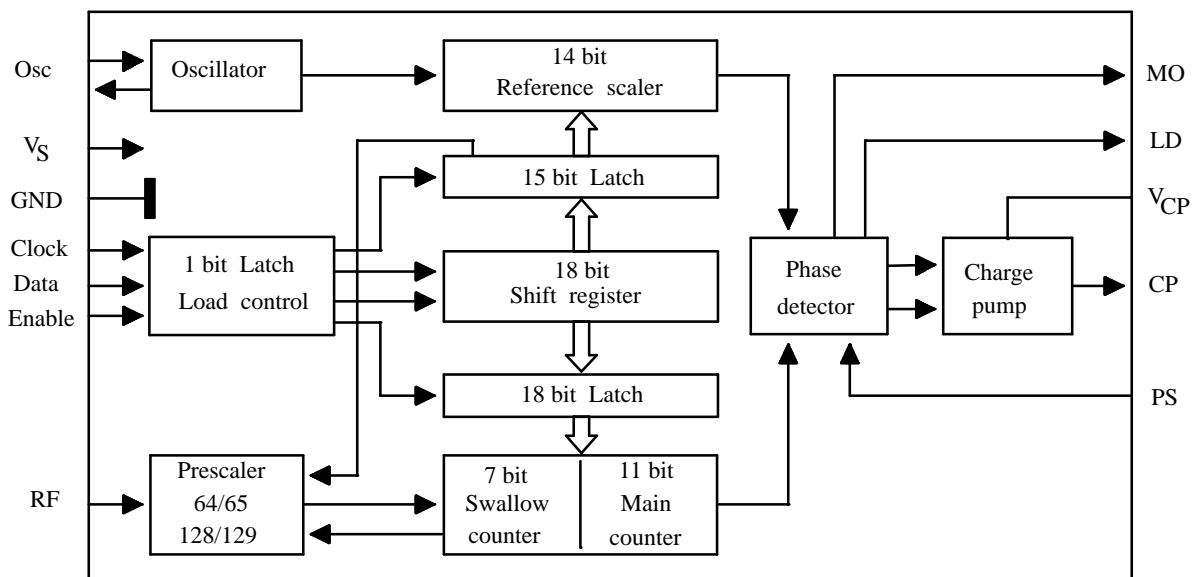
The charge pump output operates as a switch with limited max. current. The requirements of the PLL loop can be determined by the external low pass filter.

The phase characteristic of the phase detector is convertible and so matchable to different frequency / tuning voltage characteristics.

Features

- Very low current consumption (typ. 3 V/7.5 mA)
- Supply voltage range 2.7 V – 5.5 V
- Max. input frequency 1.1 GHz
- Programmable prescaler 64/65 or 128/129
- Controlled by 3-wire-bus with f_{clock} up to 500 kHz
- Status output for PLL lock/unlock condition
- Very fast phase detector
- SO-16 as well as SSO-20 package
- ESD protection in accordance with MIL-STD. 883 method 3015 class 2

Block Diagram / Applications



93 7785 e

Pin Description – SO-16

Pin	Symbol	Function
1	OSC in n.c.	Oscillator input Not connected
2	OSC out	Oscillator output
3	V _{cp}	Charge pump supply voltage
4	V _s	Supply voltage
5	CP	Charge pump output
6	GND	Ground
7	LD n.c.	Lock-detector output Not connected
8	RF in	VCO input
9	Clock n.c.	3-wire-bus clock Not connected
10	Data	3-wire-bus data
11	Enable	3-wire-bus enable
12	PS	Phase inverting input
13	n.c.	Not connected
14	M out	Monitor output for f _p and f _r
15	n.c. (PCP) n.c.	Not connected Not connected
16	n.c. (PCR)	Not connected

Pin Description – SSO-20

Pin	Symbol	Function
1	OSC in n.c.	Oscillator input Not connected
2	OSC out	Oscillator output
3	OSC out	Oscillator output
4	V _{cp}	Charge pump supply voltage
5	V _s	Supply voltage
6	CP	Charge pump output
7	GND	Ground
8	LD n.c.	Lock-detector output Not connected
9	RF in	VCO input
10	RF in	VCO input
11	Clock n.c.	3-wire-bus clock Not connected
12	Clock n.c.	3-wire-bus clock Not connected
13	Data	3-wire-bus data
14	Enable	3-wire-bus enable
15	PS	Phase inverting input
16	n.c.	Not connected
17	M out	Monitor output for f _p and f _r
18	n.c. (PCP)	Not connected
19	n.c.	Not connected
20	n.c. (PCR)	Not connected

Absolute Maximum Ratings

Parameters	Symbol	Value	Unit
Supply voltage	V _S	-0.3 to 6	V
RF input	V _{RF}	V _S	V
Oscillator input voltage	V _{OscI}	1	V
Oscillator output voltage	V _{OscO}	1.5	V
Bus input voltage	V _{BUS}	6	V
Phase select input voltage	V _{PS}	6	V
Charge pump input voltage	V _{CP}	6	V
Ambient temperature	T _{amb}	-40 to 85	°C
Storage temperature	T _{stg}	-40 to 125	°C
Thermal resistance junction-ambient	R _{thJA}	110 140	K/W
Operating range			
Supply voltage	V _S	2.7 to 5.5	V
Ambient temperature	T _{amb}	-40 to 80	°C

Electrical Characteristics

$T_{amb} = 25^{\circ}\text{C}$, $V_S = 2.7$ to 5.5 V, unless otherwise specified.

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
DC Supply						
Supply voltage	1	V_S	2.7		5.5	V
Supply current	$V_S = 3$ V	I_S		7.5		mA
Supply voltage CP		V_{CP}	V_S		5.5	V
Supply current CP	$V_{CP} = 5$ V, PLL	I_{CP}		1		μA
RF input						
Input voltage $f_i = 200$ to 1100 MHz	$R_S = 50 \Omega$ *) $R_S = 50 \Omega$ *)	V_{imin} V_{imax}		20 200		mV _{RM} mV _{RMSS}
Frequency range		f_{imin} f_{imax}	1100	50 1250		MHz MHz
Scaling factor prescaler		S_{PSC}		64/128		
Scaling factors main counter		S_M	2		2047	
Scaling factors swallow counter		S_S	0		127	
Reference oscillator						
Input voltage	$R_S = 50 \Omega$ *) $R_S = 50 \Omega$ *)	V_{imin} V_{imax}		20 200		mV _{RMS} mV _{RMS}
Frequency range		f_{imin} f_{imax}		0,1 16		MHz MHz
Scaling factor reference counter		S_R	4		16383	
3-wire bus (Clock, Data, Enable) and PS						
High-input voltage		V_{iH}	1.5	0.9		V
Low-input voltage		V_{iL}	0		0.4	V
High-input current		I_{iH}			5	μA
Low-input current		I_{iL}	-5			μA
Monitor output (emitter follower)						
High-output voltage	$V_S = 3$ V	V_{iH}	2.1	2.2		V
Low-output voltage	$I_{MO} = 0.5$ mA	V_{iL}		1.8	1.9	V
Charge pump output						
Source current	$V_{CP} = 5$ V	I_{source}		-1		mA
Sink current		I_{sink}		1		mA
Leakage current	$V_{CP} = 5$ V	I_{leak}		± 5		nA
Lock detector output (open collector)						
Saturation voltage	$I_{LD} = 1$ mA	V_{sat}		0.2	0.4	V
Cut-off current	$V_{LD} = 5$ V	I_{cut}			1	μA

*) RMS voltage at 50Ω

Functional Description

Reference and programmable counter can be programmed by the 3-wire bus (Clock, Data and Enable). The Data Signal is transferred bit by bit during the rising edge into the shift register, starting with the MSB-bit. As

soon as the enable signal is in high condition the contents of the shift register will be taken over either into the 15 bit reference counter latch (C = H) or into the 18 bit latch of the programmable counter (C = L).

Reference Counter (15-bit shift register)

LSB														MSB	
C	R0	R1	R2	R3	R4	R5	R6	R7	R8	R9	R10	R11	R12	R13	PSC

C: Control bit High

PSC: Prescaler scaling factor bit: High – 64/65
 Low – 128/129
 $S_{PSC} = 64$ or 128

R₀ to R₁₃:

These bits are setting the reference counter S_R
 $S_R = R_0 \cdot 2^0 + R_1 \cdot 2^1 + \dots + R_{12} \cdot 2^{12} + R_{13} \cdot 2^{13}$
 allowed scaling factors for S_R : 2 to 16383

Programmable Counter (18bit shift register)

LSB																	MSB	
C	S0	S1	S2	S3	S4	S5	S6	M0	M1	M2	M3	M4	M5	M6	M7	M8	M9	M10

C: Control bit Low

S₀ to S₆:

These bits are setting the swallow counter S_S .
 $S_S = S_0 \cdot 2^0 + S_1 \cdot 2^1 + \dots + S_5 \cdot 2^5 + S_6 \cdot 2^6$
 allowed scaling factors for S_S : 0 to 127, $S_S < S_M$

M₀ to M₁₀:

These bits are setting the main counter S_M .
 $S_M = M_0 \cdot 2^0 + M_1 \cdot 2^1 + \dots + M_9 \cdot 2^9 + M_{10} \cdot 2^{10}$
 allowed scaling factors for S_M : 2 to 2047

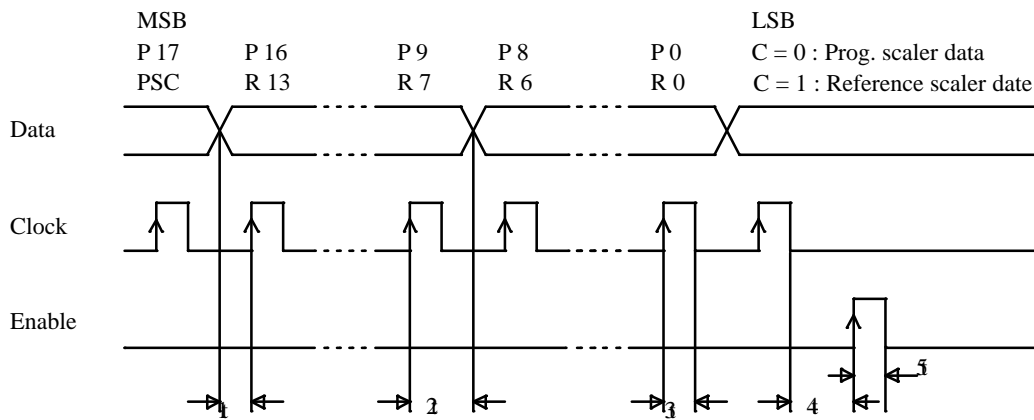
Total scaling factor S_P of the programmable counter

$$S_P = (S_{PSC} \cdot S_M) + S_S \quad \text{Condition: } S_S < S_M$$

VCO-Frequency

$$f_{VCO} = ((S_{PSC} \cdot S_M) + S_S) \cdot f_{RefOsc} / S_R$$

Timing 3-Wire-Bus



All times $t_1 \dots t_5 >= 1$

93 7787 e

Phase Detector Polarity

The polarity of the phase detector can be changed with the PS input. Depending on the PS input level the charge pump current will also be inverted. The monitor output

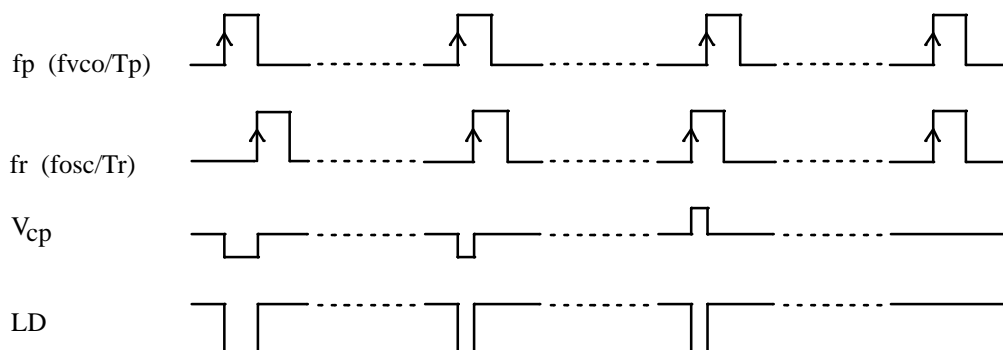
signal MO (emitter follower output with ECL level) will be switched over from f_P to f_R simultaneously.

	PS = High or Open		PS = Low	
	CP	MO	CP	MO
$f_R > f_P$	I_{sink}	f_R	I_{source}	f_P
$f_R < f_P$	I_{source}	f_R	I_{sink}	f_P
$f_R = f_P$	0	f_R	0	f_P

Depending on the VCO frequency versus tuning voltage characteristic the PS input has to be programmed as follows:

For increasing tuning voltage and increasing frequency: PS = High or open
decreasing frequency: PS = Low.

Pulse Diagram Phase and Lock Detector



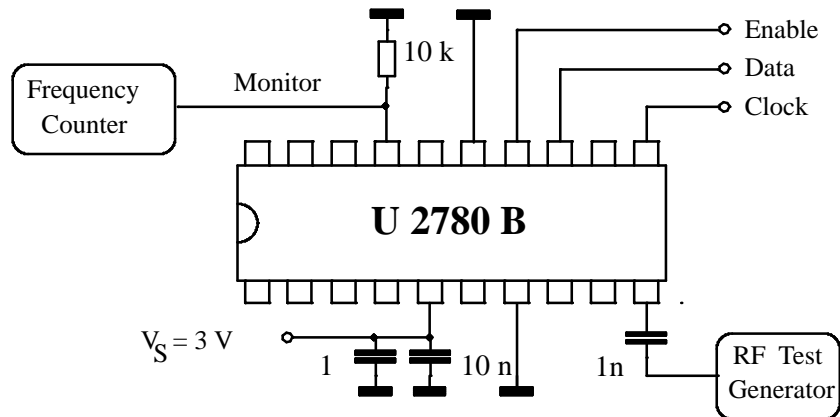
93 7786 e

The LD output is in unlocked condition at low level and the pulse width is in reference to the phase respectively frequency difference at the phase detector. If the phase de-

tor output pulses are smaller than 100 ns the LD output goes high and indicates "lock" condition.

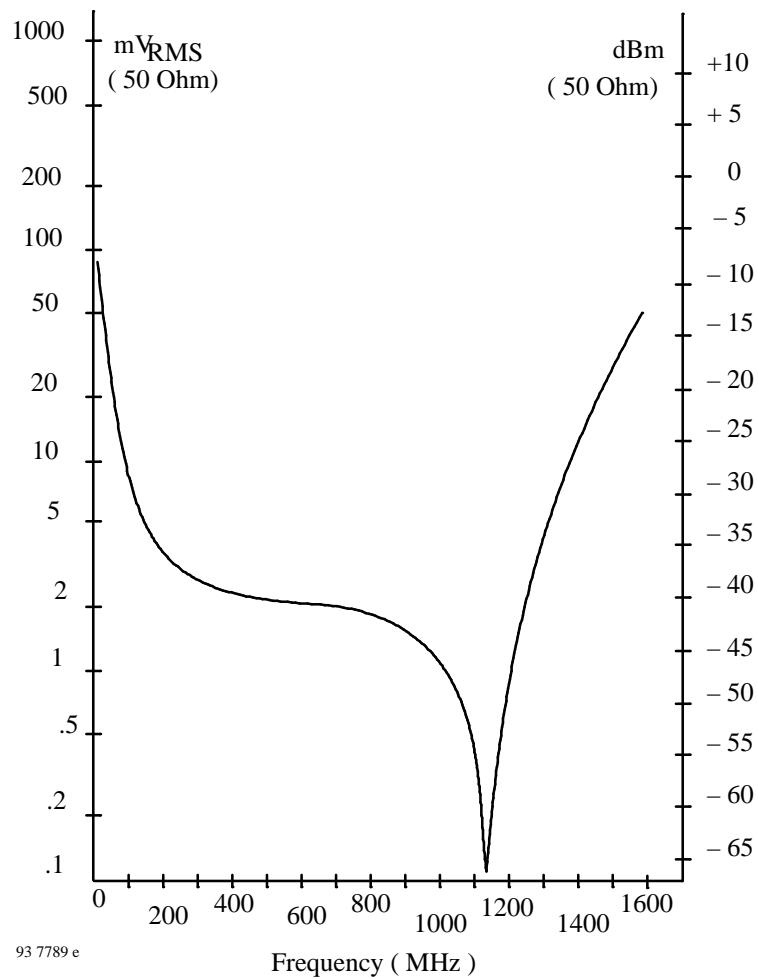
Test Circuit

Input sensitivity



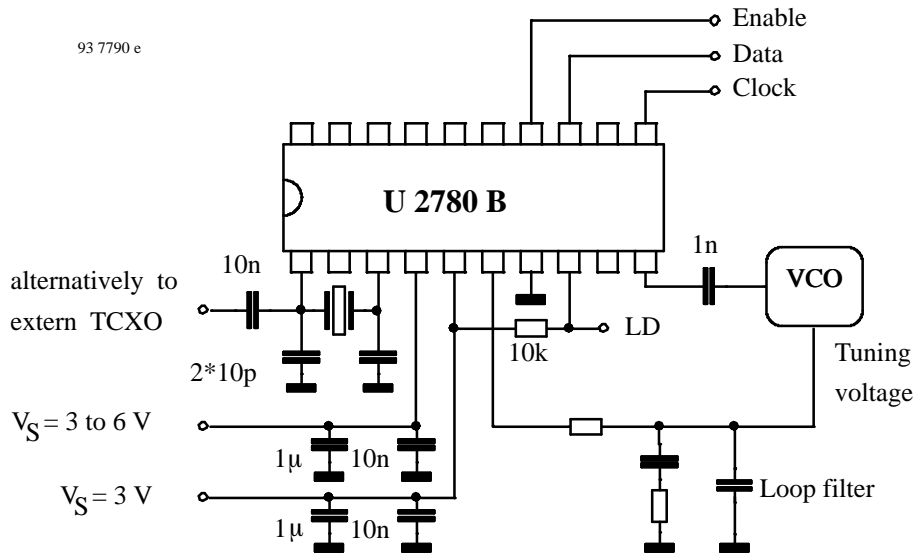
93 7788 e

Typical Input Sensitivity



93 7789 e

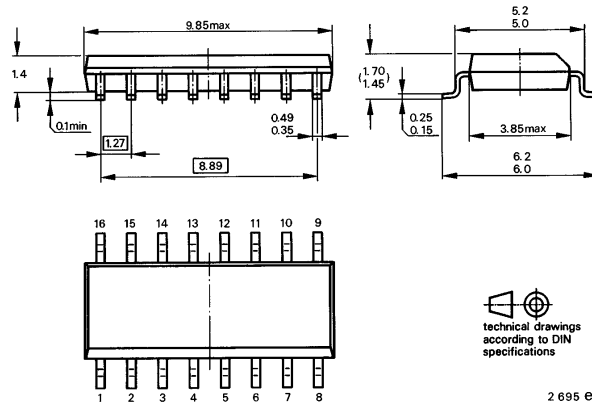
Application Circuit



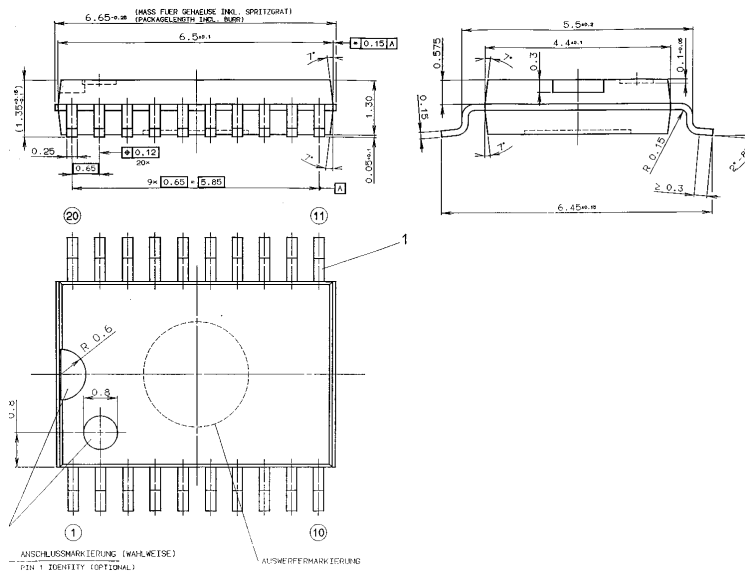
U2780B-AFP

Dimensions in mm

Package: SO-16 (U 2780 B-AFP)



Package: SSO-20 (U 2780 B-AFS)



Ozone Depleting Substances Policy Statement

It is the policy of **TEMIC TELEFUNKEN microelectronic GmbH** to

1. Meet all present and future national and international statutory requirements.
2. Regularly and continuously improve the performance of our products, processes, distribution and operating systems with respect to their impact on the health and safety of our employees and the public, as well as their impact on the environment.

It is particular concern to control or eliminate releases of those substances into the atmosphere which are known as ozone depleting substances (ODSs).

The Montreal Protocol (1987) and its London Amendments (1990) intend to severely restrict the use of ODSs and forbid their use within the next ten years. Various national and international initiatives are pressing for an earlier ban on these substances.

TEMIC TELEFUNKEN microelectronic GmbH semiconductor division has been able to use its policy of continuous improvements to eliminate the use of ODSs listed in the following documents.

1. Annex A, B and list of transitional substances of the Montreal Protocol and the London Amendments respectively
2. Class I and II ozone depleting substances in the Clean Air Act Amendments of 1990 by the Environmental Protection Agency (EPA) in the USA
3. Council Decision 88/540/EEC and 91/690/EEC Annex A, B and C (transitional substances) respectively.

TEMIC can certify that our semiconductors are not manufactured with ozone depleting substances and do not contain such substances.

We reserve the right to make changes to improve technical design and may do so without further notice.

Parameters can vary in different applications. All operating parameters must be validated for each customer application by the customer. Should the buyer use TEMIC products for any unintended or unauthorized application, the buyer shall indemnify TEMIC against all claims, costs, damages, and expenses, arising out of, directly or indirectly, any claim of personal damage, injury or death associated with such unintended or unauthorized use.

TEMIC TELEFUNKEN microelectronic GmbH, P.O.B. 3535, D-74025 Heilbronn, Germany
Telephone: 49 (0)7131 67 2831, Fax number: 49 (0)7131 67 2423